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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,139	06/13/2001	Honchin En	Q63452	6279

23373 7590 04/18/2005

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/787,139	EN ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13,22-26,32,37,38 and 42-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13 and 48-51* is/are allowed.

6)☒ Claim(s) *22-26,32,37,38,40-46 and 52-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 May 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "wherein said roughened surface comprises a primary anchor and a secondary anchor" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 24 and 57 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,258,094 (hereafter Furui).

Examiner notes the limitation that the upper-layer conductor circuit be built "by a build up process" is a process limitation in a device claim and thus is considered only to the extent to which said limitation impact the structure of the device. Furthermore, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)).

Additionally, Examiner notes that the terms "upper" and "lower" are dependent on a particular orientation of the device and are not intrinsic properties. Thus any direction could be considered to be "upper" or "lower" as long as a consistent scheme is utilized.

Furui discloses, referring to figures 11-18, a printed circuit board comprising a substrate board (14) formed with a lower layer conductor circuit (63) and built thereon an upper layer conductor circuit (64) through the intermediary of an inter layer resin insulating layer (9), with said upper layer conductor circuit and said lower layer conductor circuit being interconnected by via holes (42, 5), wherein said lower layer conductor circuit has a roughed surface, said upper layer conductor circuit comprises an electroless plated film and an electroplated film (see col. 5, lines 10-15) said interlayer

resin insulating layer is provided with a roughened surface, with said electroless plated film being complementary to said roughened surface, and said interlayer resin insulating layer and said via holes are provided with the same electroless plated film (see col. 5, lines 10-15), with said electroless plated film formed on the bottoms of said via holes having a thickness equal to 50 to 100% of the thickness of said electroless plated film on said interlayer resin insulating layer and said lower-layer conductor circuit and said electroless plated film formed on the bottom of said via hole are connected through said roughened surface of said lower-layer conductor (see fig. 16) [claim 24] wherein the via holes have a diameter of 80 μm or less [claim 55].

Claims 32, 37, 38, 40-45, and 57 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,699,613 (Chong).

Chong discloses, referring to figures 1-7, a multilayer printed circuit board comprising a core board (1) having on both sides conductor circuits (12, 14) and, over said conductor circuit, buildup wiring layers comprising alternating an interlayer resin insulating layer (23) and a conductor layer (31) thereon, wherein the conductor layers are interconnected by via holes (26, 29), wherein said core board comprises a copper-clad laminate, said conductor circuit comprises a copper foil of said copper-clad laminate and a plated metal layer, wherein the thickness of said conductor circuit is not greater by more than 10μm than the thickness of said conductor layer on said interlayer resin insulating layer [claim 32], wherein said conductor circuit on said core board is a conductor layer interconnected with a plated through hole (38, see fig. 9) [claim 57]

Additionally, Chong discloses, referring to figures 1-7, a multilayer printed circuit board comprising a core board (1) having on both sides conductor circuits (12, 14) and over each of said conductor circuits, a buildup wiring layer comprising alternating an interlayer resin insulating layer (23) and a conductor layer (31) thereon wherein said conductor layers are interconnected by via holes (26, 29), wherein said core board is a copper-clad laminate (see col. 3, lines 30-45) and is provided with plated through holes (16), said conductor circuit comprise a copper foil of said coppe-clad laminate and a plated film said via holes are formed immediately over said plated through holes in the manner of plugging the through holes in said plated through holes and are interconnected with said plated through holes [claims 37, 40, 41, 42], wherein the through holes have a diameter of not more than 200 μm (see col. 4, lines 30-50) [claim 38], which comprises bumps (44) formed immediately above sad plated through holes [claim 43], wherein said lower layer via holes are filled with metal (31) [claim 44], wherein the valleys of said via holes are filled with a conductive paste (32) [claim 45], wherein valleys of said lower layer via holes are filled with a resin (32) [claim 46].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 22, 23, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4,642,163 (hereafter Greschner) in view of US 5,200,271 (Kosaka).

Greschner discloses, referring to figures 1A-1F, a printed circuit board comprising a resin insulating substrate board (1) formed with a roughened surface and thereon a conductor circuit (7) comprising an electroless plated film, wherein said electroless plated film is formed on a surface of said roughend surface (see fig. 1F) and has a stress of 0 to +10 kg/mm2 (see col. 2, lines 40-50). Greschner does not

specifically disclose an additionally electroplated film [claim 22]. However, it is well known in the art to electroplate over an electroplated film to quickly build up the conductor to the desired height as evidenced by Kosaka (see col. 7, lines 5-55). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to add an electroplated film over the electroless plated film of Greschner as is well known in the art and evidenced by Kosaka. The motivation for doing so would have been to reduce the time needed to buildup the conductor to the required thickness, thus reducing the processing time of the device. Moreover, the modified invention of Greschner teaches wherein said electroless plating solution is formed from an electroless plating solution comprising tartaric acid or a salt thereof (see col. 6, lines 15-20) [claim 52]

Similarly, Greschner discloses a printed circuit board comprising a resin insulating substrate (1) formed with a roughened surface and built thereon by semi-additive process a conductor circuit comprising at least an electroless plated film (7), wherein said roughened surface comprises concave areas and convex area, and said electroless plated film is complementary to a surface of said roughened surface with said electroless plated film in convex areas of said roughened surface being relatively greater in thickness than said electroless plated film in concave area of said roughened surface (see figure 1F). Greschner does not specifically disclose an additionally electroplated film [claim 23]. However, it is well known in the art to electroplate over an electroplated film to quickly build up the conductor to the desired height as evidenced by Kosaka (see col. 7, lines 5-55). Therefore, it would have been obvious, to one having

ordinary skill in the art, at the time of invention, to add an electroplated film over the electroless plated film of Greschner as is well known in the art and evidenced by Kosaka. The motivation for doing so would have been to reduce the time needed to buildup the conductor to the required thickness, thus reducing the processing time of the device.

Claims 25, 26, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greschner in view of Kosaka as applied to claim 22 above, and further in view of US 5,589,255 (hereafter Suzuki).

Greschner in view of Kosaka discloses the invention as described above except it does not specifically teach wherein said electroless plated film is a copper film and comprises one metal species selected from the group consisting of nickel, iron and cobalt [claims 25, 56], wherein the proportion of said at least one metal species selected from the group consisting of nickel, iron and cobalt is 0.1 to 0.5 weight % [claim 26]. Suzuki discloses, referring to figure 1C, a printed circuit board comprising a resin insulating substrate board (2) and thereon a conductor circuit (3) comprising at least an electroless plated film (see col. 6, lines 35-40), wherein said electroless plated film is a copper film and comprises one metal species selected from the group consisting of nickel, iron and cobalt (see col. 4, lines 5-10) [claims 25, 56], wherein the proportion of said at least one metal species selected from the group consisting of nickel, iron and cobalt is 0.1 to 0.5 weight % (see col. 3, lines 50-60) [claim 26] . Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use

the conductor taught by Suzuki in the invention of Greschner as modified by Kosaka. The motivation for doing so would have been to increase the peel strength of the conductor, thus making the device more resistant to failure.

Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furui in view of Greschner.

Furui discloses the calimed invention as described above with respect to claim 24 except Furui does not specifically state that the electroless plating solution is formed from an electroless plating solution comprising tartaric acid or a salt thereof [claim 54]. However, it is well known in the art to use tartaric acid or slats thereof for electroless plating solutions as evidenced by Greschner (see col. 6, lines 15-20). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the solution taught by Greschner in the invention of Furui. The motivation for doing so would have been to easily manufacture the copper layer. Moreover, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Allowable Subject Matter

The indicated allowability of claim 43 and 46 is withdrawn in view of the newly discovered reference(s) as cited. Rejections based on the newly cited reference(s) are as cited above.

Claims 9-13 and 48-51 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: Claims 9, 11, and 12 state the limitation "wherein said copper film comprises an electroplated layer and has properties that (a) its crystallinity is such that the X-ray diffraction half-width of the (331) plane of copper is less than 0.3 deg". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art.

Response to Arguments

Applicant's arguments with respect to claims 22, 23, 25, 26, 32, 37, 38, 40-42, 45, 52, and 54-56 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 10 Janurary 2005, regarding claims 24 and 57, have been fully considered but they are not persuasive. Applicants allege that the instantly claimed invention distinguishes over the prior art because the instantly claimed invention is formed by a build up process and the invention of Furui is formed by a heat and press lamination process. However, as noted above, this is a process limitation in a device claim and thus is considered only to the extent to which said limitation impact the structure of the device. Furthermore, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product. (*In re Thorpe,* 227 USPQ 964, 966 (Fed. Cir. 1985)). Applicants further assert "the electroless plated conductive layer 64 of Furui does not comprise an electroplated film". However as clearly stated in Furui:

> *"Then a 4th conductive layer 64 and a lower-most conductive layer 67 of copper are formed on the entire surface of the plate including photovia holes 42 in thickness (sic) ranging from 12 μm to 18μm by the known electroless plating* ***and*** *electroplating methods to thus connect the 5th conducive layer 65 and the 4th conductive layer 64 (FIG. 12A)" (emphasis added).*

Thus, there can be no doubt that the layer 64 of Furui indeed comprises electroless plating **and** electroplating.

Applicants additionally assert that the conductor layer 65 does not have a roughened surface. However, this point is moot as the examiner has not relied upon layer 65 to meet Applicants claim to a lower-layer conductor having a roughened surface in the instant rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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